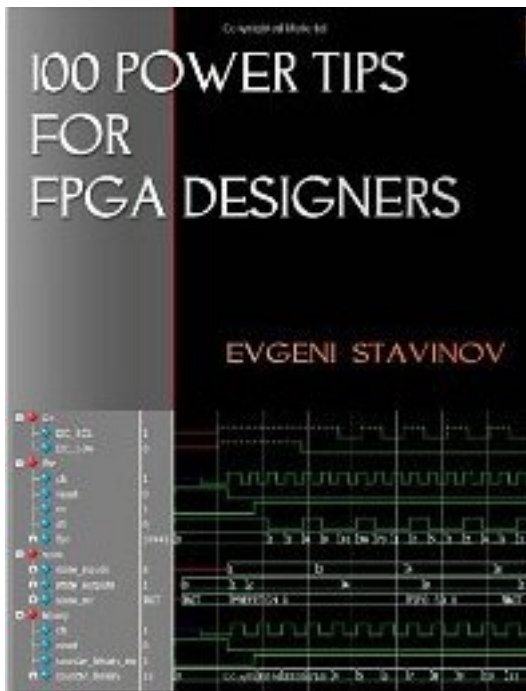


100 Power Tips For FPGA Designers



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This book is a collection of short articles on various aspects of FPGA design: synthesis, simulation, porting ASIC designs, floorplanning and timing closure, design methodologies, performance, area and power optimizations, RTL coding, IP core selection, and many others. The book is intended for system architects, design engineers, and students who want to improve their FPGA design skills. Both novice and seasoned logic and hardware engineers can find bits of useful information. This book is written by a practicing FPGA logic designer, and contains a lot of illustrations, code examples, and scripts. Rather than providing information applicable to all FPGA vendors, this book edition focuses on Xilinx Virtex-6 and Spartan-6 FPGA families. Code examples are written in Verilog HDL.

作者介绍:

Evgeni Stavinov is a longtime FPGA user with more than 10 years of diverse design experience. Before becoming a hardware architect at SerialTek LLC, he held different engineering positions at Xilinx, LeCroy and CATC. Evgeni holds MS and BS degrees in electrical engineering from University of Southern California and Technion - Israel Institute of Technology. Evgeni is a creator of OutputLogic.com, a portal that offers different online productivity tools.

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书评

值得在茶余饭后读一读，就像读杂志一样。很多问题仅仅点到而止，没有直击命门，不过仅仅是学到有这些问题也是值得的。书真的很新，连Zync都有提到！越往后错字越多，看来从blog转写书还是不灵，估计也是没钱好好review就匆忙上架了。有不少方法论的东西，遇到问题可以参...

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