Phase-Locked Loop Synthesizer Simulation

Phase-Locked Loop Synthesizer Simulation_下载链接1_

著者:Bianchi, Giovanni

出版者:McGraw-Hill

出版时间:2005-4

装帧:

isbn:9780071453714

Phase locked loops (PLLs) are electronic circuits that ensure that a communications

signal stays locked on a given frequency. Their design is crucial to the workings of wireless communications systems. Virtually all transceivers use PLLs to synthesize the stable, high frequency oscillations necessary for radio & wireless. This book describes how to calculate PLL performances by using standard mathematical or circuit analysis programs. Theoretical descriptions are limited to the minimum needed to explain how to perform calculations. Although presented methods of analysis can be implemented with many commercial programs, their description always refers to Mathcad and SIMetrix.

作者介绍:

目录:

标签

评论

Phase-Locked Loop Synthesizer Simulation_下载链接1_

书评

Phase-Locked Loop Synthesizer Simulation_下载链接1_