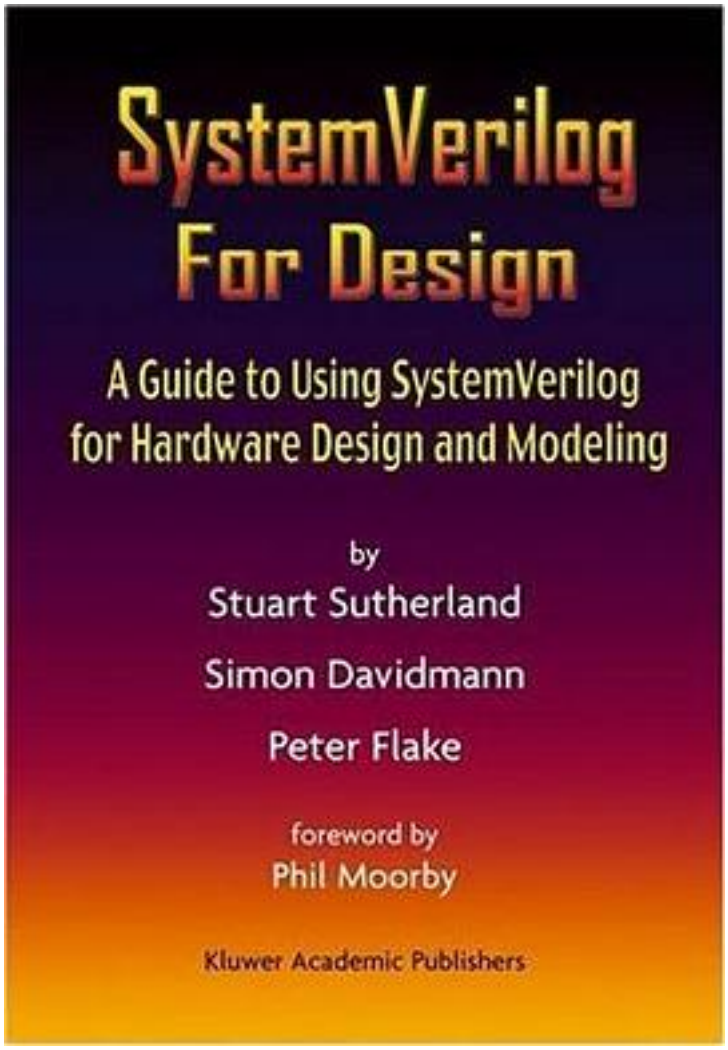
SystemVerilog For Design



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SystemVerilog is a rich set of extensions to the IEEE 1364-2001 Verilog Hardware Description Language (Verilog HDL). These extensions address two major aspects of HDL based design. First, modeling very large designs with concise, accurate, and intuitive code. Second, writing high-level test programs to efficiently and effectively verify these large designs. This book, SystemVerilog for Design, addresses the first aspect of the SystemVerilog extensions to Verilog. Important modeling features are presented, such as two-state data types, enumerated types, user-defined types, structures, unions, and interfaces. Emphasis is placed on the proper usage of these enhancements for simulation and synthesis. A companion to this book, SystemVerilog for Verification, covers the second aspect of SystemVerilog.

作者介绍:

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标签

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评论

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书评

这本书主要是从硬件方面来对SV进行介绍的，也就是介绍SV在硬件实现方面的强大功能。
很好的一点是，它是对照着verilog来介绍的。同样的功能，Verilog会怎样处理，而SV又会怎样处理，这样能够很容易地加深对SV的理解。
看这本书用了我2天的时间。当然，只是粗略读了一遍，但是...

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