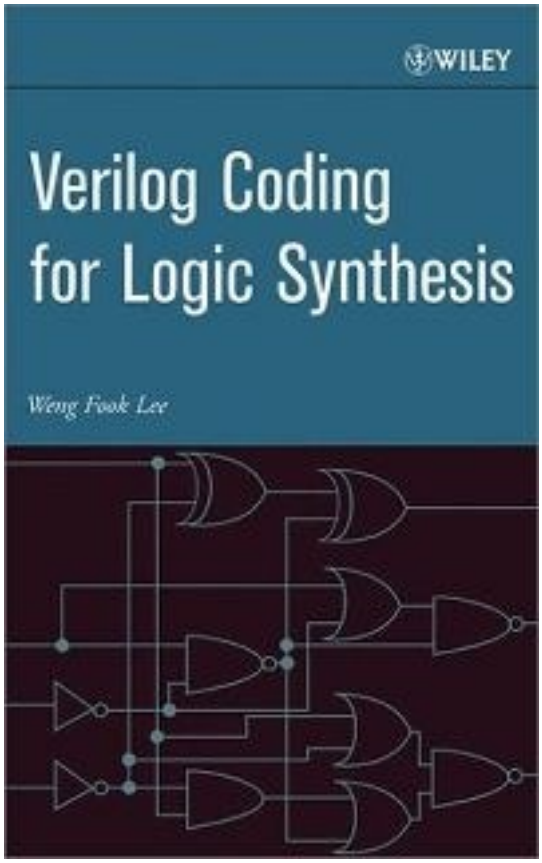
Verilog Coding for Logic Synthesis



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著者:Weng Fook Lee

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Provides a practical approach to Verilog design and problem solving. Bulk of the book deals with practical design problems that design engineers solve on a daily basis. Includes over 90 design examples. There are 3 full scale design examples that include specification, architectural definition, micro-architectural definition, RTL coding, testbench coding and verification. Book is suitable for use as a textbook in EE

departments that have VLSI courses

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