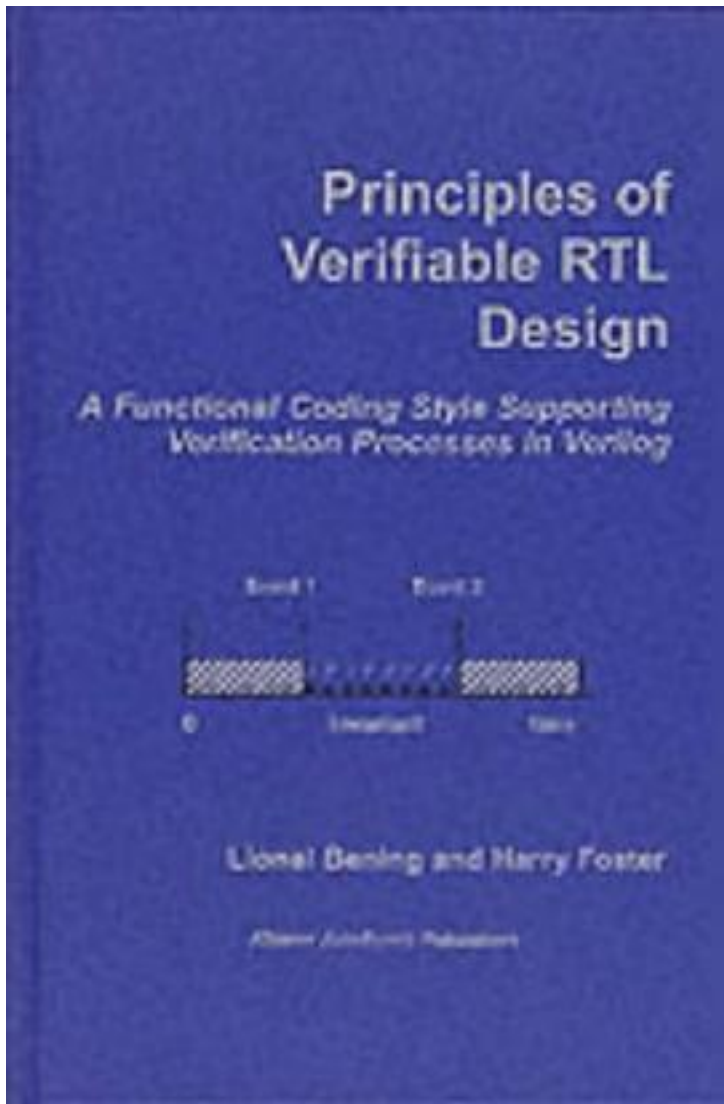


Principles of Verifiable RTL Design - A Functional Coding Style Supporting Verification Processes



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著者:Lionel Bening

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Principles of Verifiable RTL Design: A Functional Coding Style Supporting Verification Processes in Verilog explains how you can write Verilog to describe chip designs at the RT-level in a manner that cooperates with verification processes. This cooperation can return an order of magnitude improvement in performance and capacity from tools such as simulation and equivalence checkers. It reduces the labor costs of coverage and formal model checking by facilitating communication between the design engineer and the verification engineer. It also orients the RTL style to provide more useful results from the overall verification process. The intended audience for Principles of Verifiable RTL Design: A Functional Coding Style Supporting Verification Processes in Verilog is engineers and students who need an introduction to various design verification processes and a supporting functional Verilog RTL coding style. A second intended audience is engineers who have been through introductory training in Verilog and now want to develop good RTL writing practices for verification. A third audience is Verilog language instructors who are using a general text on Verilog as the course textbook but want to enrich their lectures with an emphasis on verification. A fourth audience is engineers with substantial Verilog experience who want to improve their Verilog practice to work better with RTL Verilog verification tools. A fifth audience is design consultants searching for proven verification-centric methodologies. A sixth audience is EDA verification tool implementers who want some suggestions about a minimal Verilog verification subset. Principles of Verifiable RTL Design: A Functional Coding Style Supporting Verification Processes in Verilog is based on the reality that comes from actual large-scale product design process and tool experience.

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