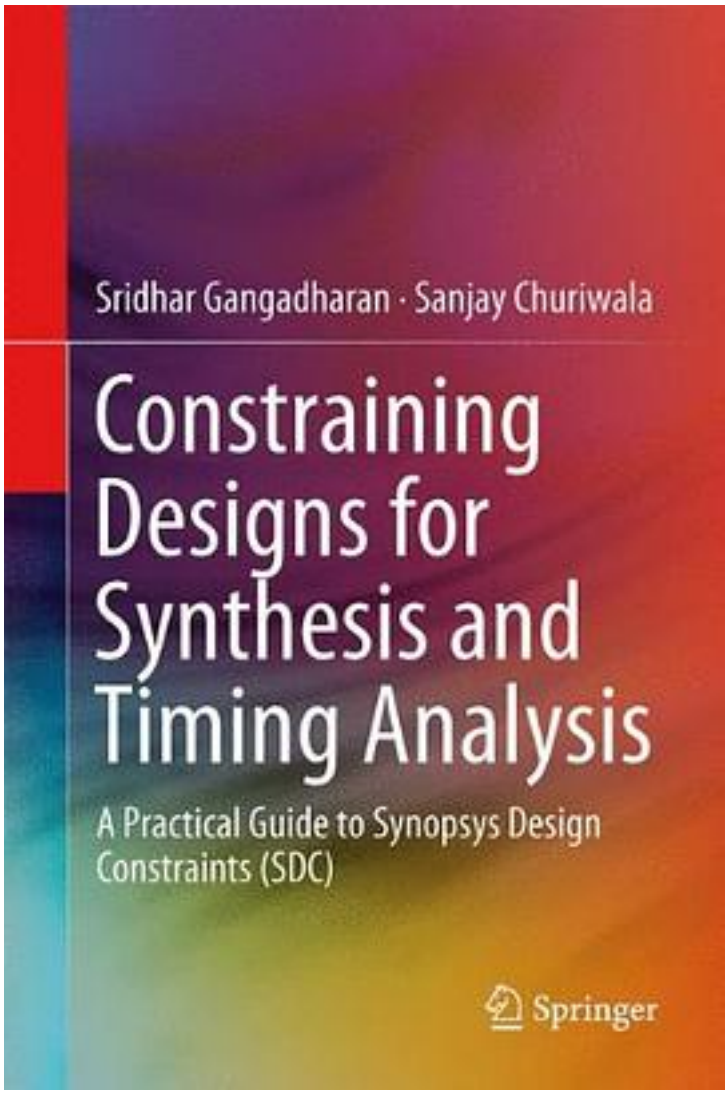
Constraining Designs for Synthesis and Timing Analysis



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This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly. Its coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

作者介绍:

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标签

STA

IC

dc

FPGA

评论

全面介绍了sdc的语法。内容不高深，但比较全面细致，我比较喜欢这种，虽然不一定能解决实际问题，但是能解决不少疑惑。

每次糊涂的时候翻一翻。但实际项目还是要灵活处理，比如arm cpu的L2 cache gated clock，它除了到L2

dataram之外还到了其他逻辑，设置其相对于别的时钟的multicycle就会变得很繁琐。因此干脆就不要create这个generated clock啦，在dataram clk端设multicycle即可。

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书评

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