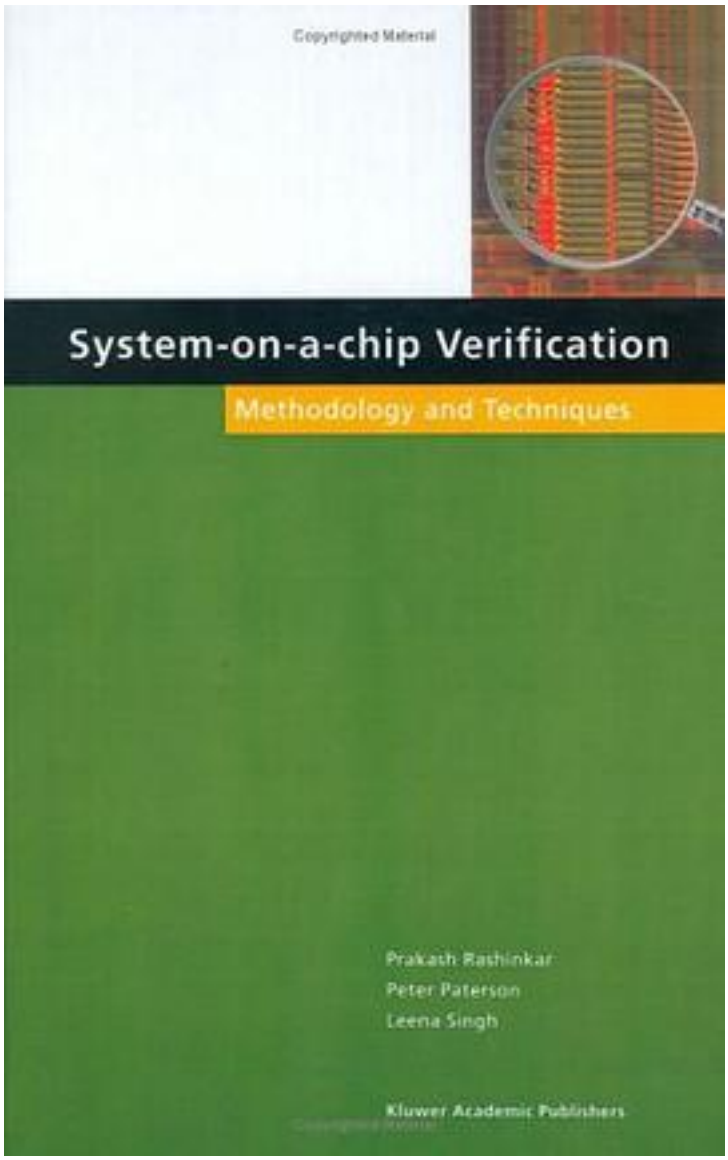
System-on-a-Chip Verification - Methodology and Techniques



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System-On-a-Chip Verification: Methodology and Techniques is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign- off. The topics covered include Introduction to the SOC design and verification aspects, System level verification in brief, Block level verification, Analog/mixed signal simulation, Simulation, HW/SW Co-verification, Static netlist verification, Physical verification, and Design sign-off in brief. All the verification aspects are illustrated with a single reference design for Bluetooth application. System-On-a-Chip Verification: Methodology and Techniques takes a systematic approach that covers the following aspects of verification strategy in each chapter: Explanation of the objective involved in performing verification after a given design step; Features of options available; When to use a particular option; How to select an option; and Limitations of the option. This exciting new book will be of interest to all designers and test professionals.

作者介绍:

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