

Fast Simulation of Computer Architectures



FAST SIMULATION OF COMPUTER ARCHITECTURES

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Chapters in Fast Simulation of Computer Architectures cover topics such as how to collect traces, emulate instruction sets, simulate microprocessors using execution-driven techniques, evaluate memory hierarchies, apply statistical sampling to simulation, and how to augment simulation with performance bound models. The chapters have been written by many of the leading researchers in the area, in a collaboration that ensures that the material is both coherent and cohesive.
Audience: Of tremendous interest to practising computer architect designers seeking timely solutions to tough evaluation problems, and to advanced upper division undergraduate and graduate students of the field. Useful study aids are provided by the problems at the end of Chapters 2 through 8.

作者介绍:

目录:

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