Computer Architecture

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Part I sets the stage, provides context, reviews some of the prerequisite topics and gives a taste of what is to come in the rest of the book. Included are two refresher-type chapters on digital circuits and components, a discussion of types of computer systems, an overview of digital computer technology, and a detailed perspective on computer system performance. Part II lays out the user's interface to computer hardware known as the instruction-set architecture (ISA). For better understanding, the instruction set of MiniMIPS (a simplified, yet very realistic, machine for which open reference material and simulation tools exist) is described. Included is a chapter on variations in ISA (e.g. RISC vs CISC) and associated cost performance tradeoffs. The next two parts cover the central processing unit (CPU). Part III describes the structure of arithmetic/logic units (ALUs) in some detail. Included are discussions of fixed- and floating-point number representations, design of high-speed adders, shift and logical operations, and hardware multipliers/dividers. Implementation aspects and pitfalls of floating-point arithmetic are also discussed. Part IV is devoted to data path and control circuits comprising the CPU. Beginning with instruction execution steps, the needed components and control mechanisms are derived. These are followed by an exposition of control design strategies, use of a pipelined data path for performance enhancement, and various limitations of pipelining due to data and control

dependencies. Part V is concerned with the memory system. The technologies in use for primary and secondary memories are described, along with their strengths and limitations. It is shown how the use of cache memories effectively bridges the speed gap between CPU and main memory. Similarly, the use of virtual memory to provide the illusion of a vast main memory is explained. Part VI deals with input/output and interfacing topics. A discussion of I/O device technologies is followed by methods of I/O programming and the roles of buses and links (including standards) in I/O communication and interfacing. Elements of processes and context switching, for exception handling or multireaded computation, are also covered. Part VII introduces advanced architectures. An overview of performance enhancement strategies, beyond simple pipelining, is presented and examples of applications requiring higher performance are cited. These are followed by design strategies and example architectures based on vector or array processing, multiprocessing, and multicomputing.

作者介绍:

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标签

体系结构

评论

偏硬；错误太多，作者主页有勘误。封面是earth simulator;

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objectively, not so bad; subjectively, it sucks…..

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书评

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