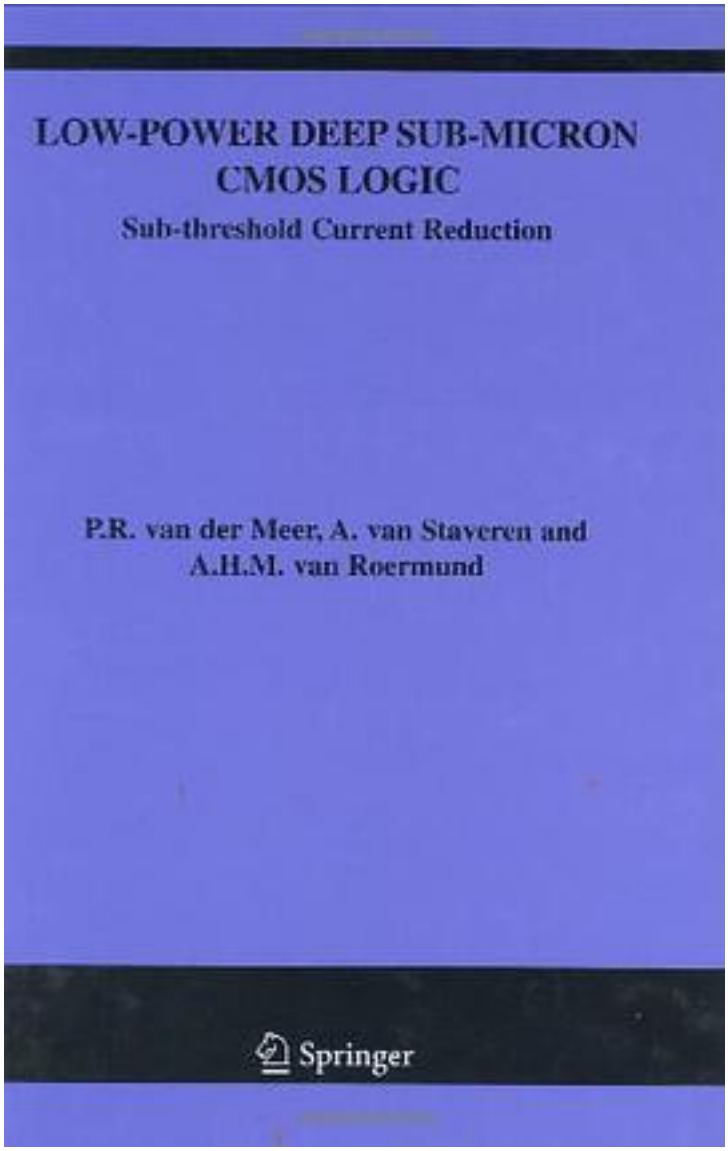
Low-Power Deep Sub-Micron Cmos Logic



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The strong interaction between the demand for increasing chip functionality and data-processing speeds, and technological trends in the integrated circuit industry, like e.g. shrinking device geometry, growing chip area and increased transistor switching speeds, cause a huge increase in power dissipation for deep sub-micron digital CMOS circuits. "Low-Power Deep Sub-micron CMOS Logic, Sub-threshold Current Reduction" classifies all power dissipation sources in digital CMOS circuits and provides for a systematic approach of power reduction techniques. A clear distinction has been made between power dissipated to perform a calculation in a certain time frame, i.e. functional power dissipation, and power dissipated even when a circuit is idle, i.e. parasitical power dissipation. The threshold voltage level forms an important link between the functional and the parasitical power dissipation. Since for high data-processing speeds the threshold voltage needs to be low, whereas for low sub-threshold leakage currents it needs to be high. The latter is extremely important for battery operated circuits in standby modes. Therefore, a separate classification of sub-threshold current reduction techniques is presented showing existing and new circuit topologies. "Low-Power Deep Sub-micron CMOS Logic, Sub-threshold Current Reduction" is a valuable book for researchers, designers as well as students in the field of low-power digital design. Power dissipation is discussed from a fundamental, quantum mechanical and a practical point of view. The theory is accompanied with practical circuit implementations and measurement results.

作者介绍:

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