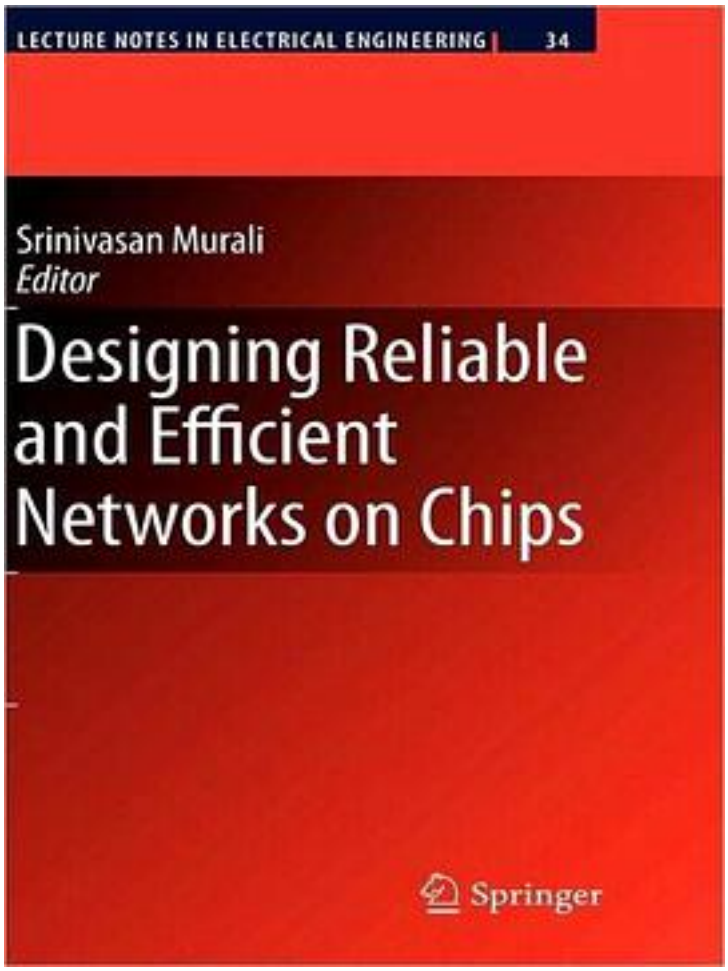
Designing Reliable and Efficient Networks on Chips



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著者:Srinivasan Murali

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About this book

Developing NoC based interconnect tailored to a particular application domain, satisfying the application performance constraints with minimum power-area overhead is a major challenge. With technology scaling, as the geometries of on-chip devices reach the physical limits of operation, another important design challenge for NoCs will be to provide dynamic (run-time) support against permanent and intermittent faults that can occur in the system. The purpose of Designing Reliable and Efficient Networks on Chips is to provide state-of-the-art methods to solve some of the most important and time-intensive problems encountered during NoC design.

Written for:

System level architects and designers, communication architecture/interconnect designers, design automation engineers, also of general interest to designers working in related fields, such as sensor, body area and automotive networks

Keywords:

* Design

* Networks on Chips

* Reliability

* Systems on Chips

* Topology

作者介绍:

CTO at iNoCs

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