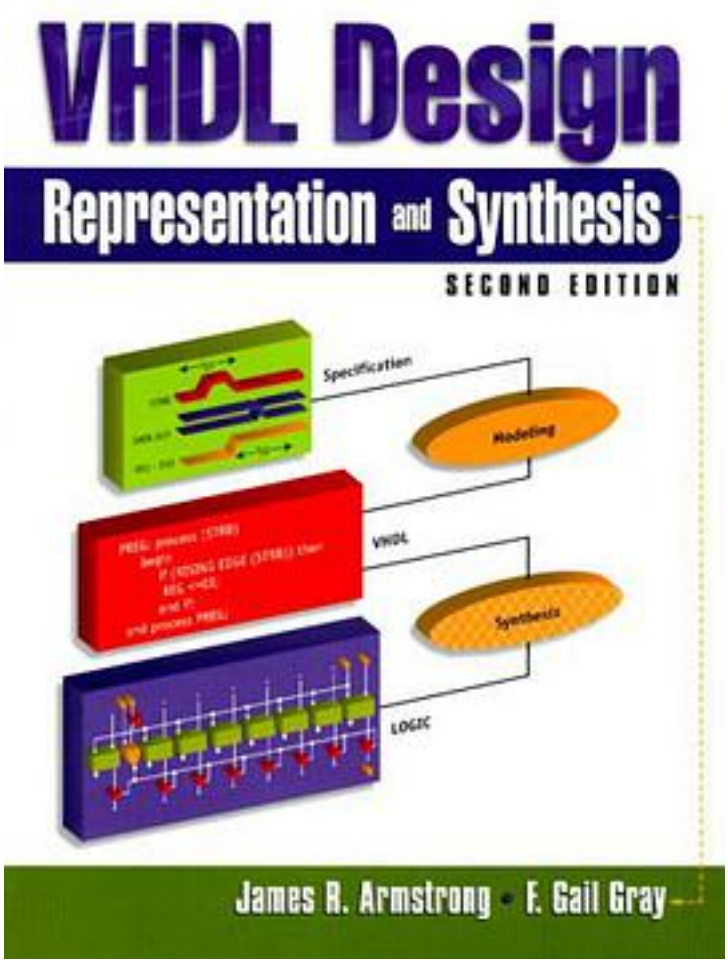
Structured Logic Design with VHDL



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For senior/graduate-level courses in Advanced Digital Design and Advanced Digital

Logic in departments of electrical engineering, computer engineering, and computer science.Intended to teach a synthesis-based approach to design using a hardware description language (i.e., VHDL), this text focuses on the synthesis process in how to translate VHDL descriptions into gate level logic. It teaches the VHDL language in detail, describes modeling at three different levels of abstraction (algorithmic, data flow, and gate level), and explains the ASIC Design Process. Illustrations of synthesis with standard cell libraries and FPGAs are given using Synopsys and Xilinx tools.

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