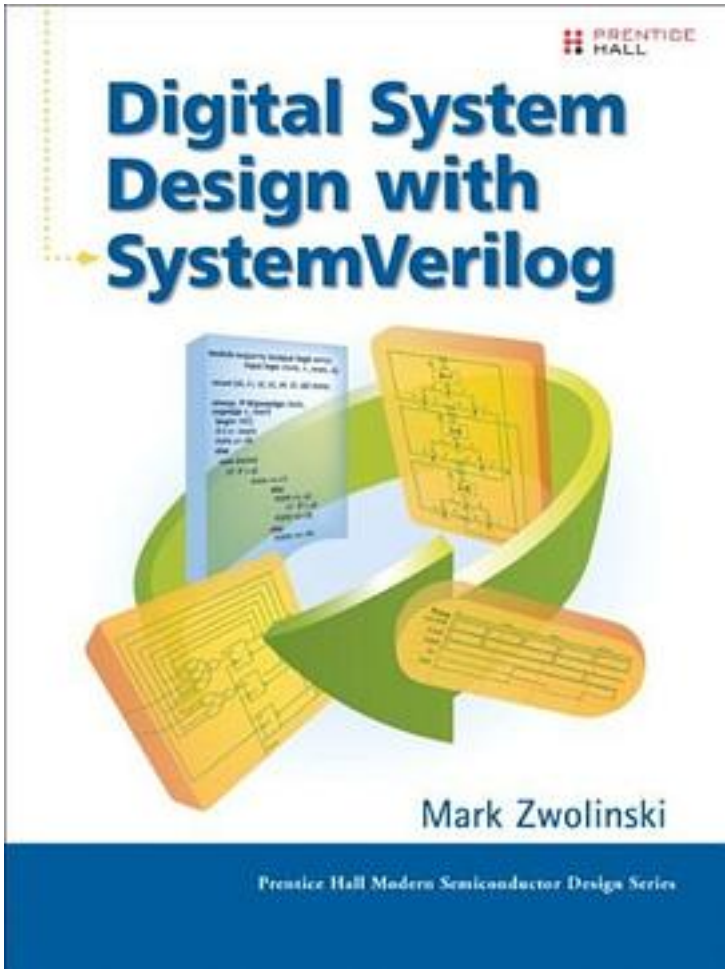
Digital System Design with SystemVerilog



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The Definitive, Up-to-Date Guide to Digital Design with SystemVerilog: Concepts, Techniques, and Code To design state-of-the-art digital hardware, engineers first

specify functionality in a high-level Hardware Description Language (HDL)-and today's most powerful, useful HDL is SystemVerilog, now an IEEE standard. Digital System Design with SystemVerilog is the first comprehensive introduction to both SystemVerilog and the contemporary digital hardware design techniques used with it. Building on the proven approach of his bestselling Digital System Design with VHDL, Mark Zwolinski covers everything engineers need to know to automate the entire design process with SystemVerilog-from modeling through functional simulation, synthesis, timing simulation, and verification. Zwolinski teaches through about a hundred and fifty practical examples, each with carefully detailed syntax and enough in-depth information to enable rapid hardware design and verification. All examples are available for download from the book's companion Web site, zwolinski.org. Coverage includes * Using electronic design automation tools with programmable logic and ASIC technologies * Essential principles of Boolean algebra and combinational logic design, with discussions of timing and hazards * Core modeling techniques: combinational building blocks, buffers, decoders, encoders, multiplexers, adders, and parity checkers * Sequential building blocks: latches, flip- flops, registers, counters, memory, and sequential multipliers * Designing finite state machines: from ASM chart to D flip-flops, next state, and output logic * Modeling interfaces and packages with SystemVerilog * Designing testbenches: architecture, constrained random test generation, and assertion-based verification * Describing RTL and FPGA synthesis models * Understanding and implementing Design-for-Test * Exploring anomalous behavior in asynchronous sequential circuits * Performing Verilog-AMS and mixed-signal modelingWhatever your experience with digital design, older versions of Verilog, or VHDL, this book will help you discover SystemVerilog's full power and use it to the fullest.

作者介绍:

是英国南安普顿大学电子与计算机科学学院的全职教授。他是Digital system Design with
VHDL一书的作者，该书已被翻译成四种语言，并被全世界的许多所大学选为教材。Zwolinski教授在技术杂志上曾发表过120多篇论文。20多年来，他一直教授大学本科生和研究生的数字设计与设计自动化等课程。

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