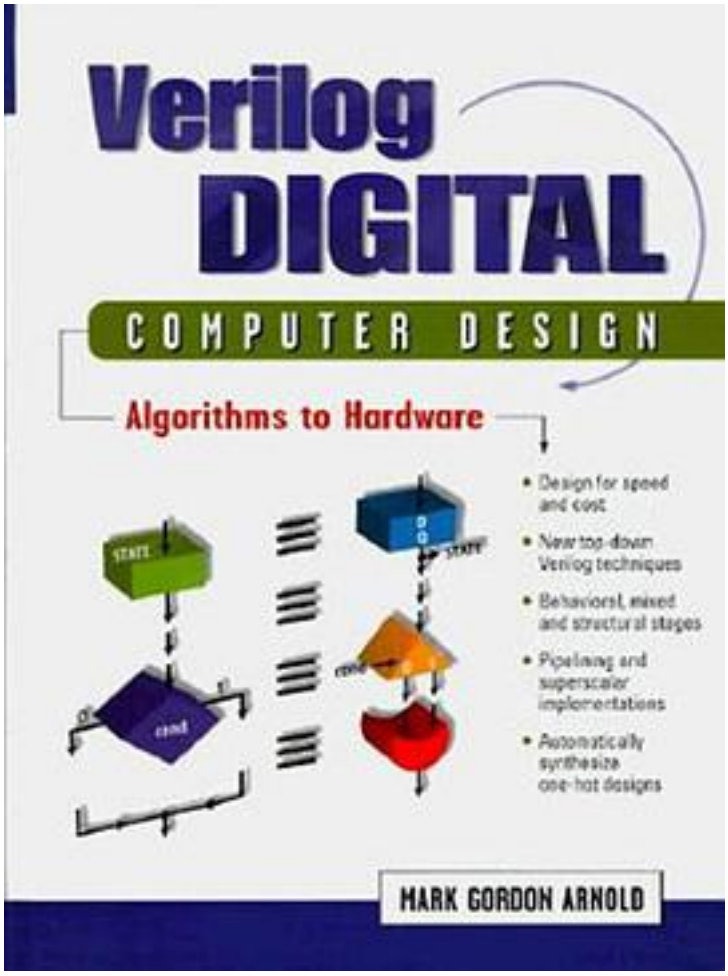
Verilog digital computer design



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For introductory-level courses in Verilog Hardware Description Language. Written by the co-developer of the Verilog Implicit To One hot (VITO) preprocessor, this text

introduces the industry standard Verilog Hardware Description Language as a new way to explore enduring concepts in digital and computer design, such as pipelining. It shows how Verilog simulation is a tool for uncovering bugs prior to hardware fabrication, and how Verilog synthesis is a tool for automatically converting source code into hardware. Ideal for designers new to Verilog, it features a consistent design framework using ASM charts, and contains many realistic, practical examples.

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