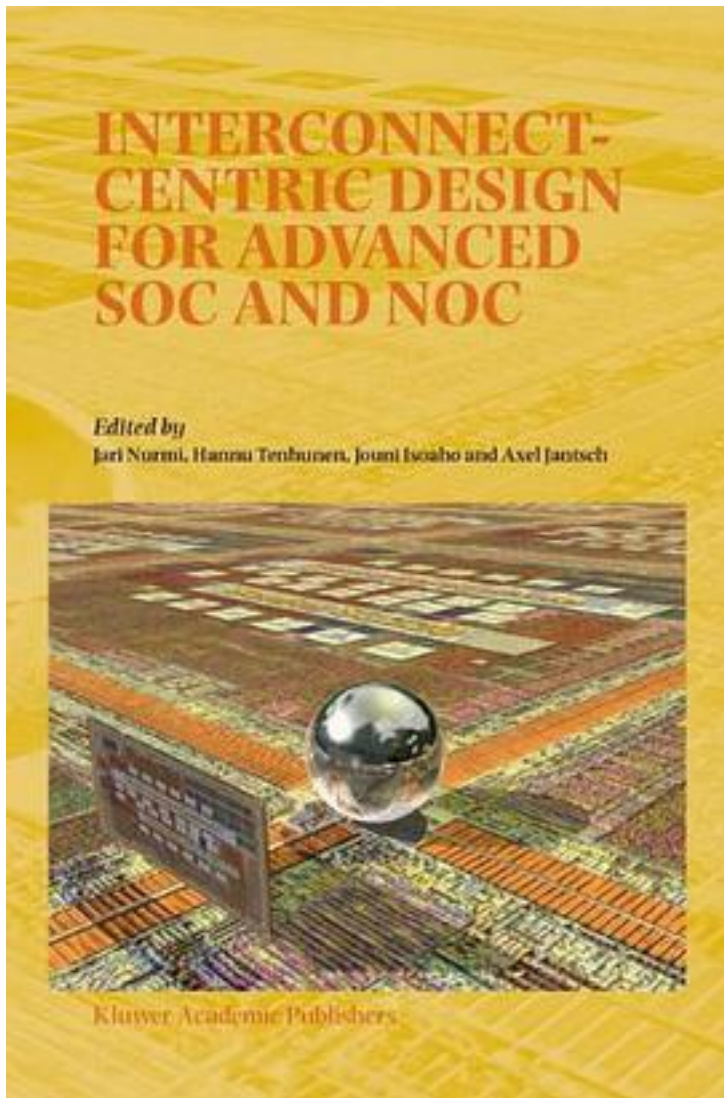


# Interconnect-Centric Design for Advanced SOC and NOC



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著者:Nurmi, Jari; Tenhunen, Hannu; Isoaho, Jouni

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In Interconnect-centric Design for Advanced SoC and NoC, we have tried to create a comprehensive understanding about on-chip interconnect characteristics, design methodologies, layered views on different abstraction levels and finally about applying the interconnect-centric design in system-on-chip design. Traditionally, on-chip communication design has been done using rather ad-hoc and informal approaches that fail to meet some of the challenges posed by next-generation SOC designs, such as performance and throughput, power and energy, reliability, predictability, synchronization, and management of concurrency. To address these challenges, it is critical to take a global view of the communication problem, and decompose it along lines that make it more tractable. We believe that a layered approach similar to that defined by the communication networks community should also be used for on-chip communication design. The design issues are handled on physical and circuit layer, logic and architecture layer, and from system design methodology and tools point of view. Formal communication modeling and refinement is used to bridge the communication layers, and network-centric modeling of multiprocessor on-chip networks and socket-based design will serve the development of platforms for SoC and NoC integration. Interconnect-centric Design for Advanced SoC and NoC is concluded by two application examples: interconnect and memory organization in SoCs for advanced set-top boxes and TV, and a case study in NoC platform design for more generic applications.

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