The Verilog® Hardware Description Language
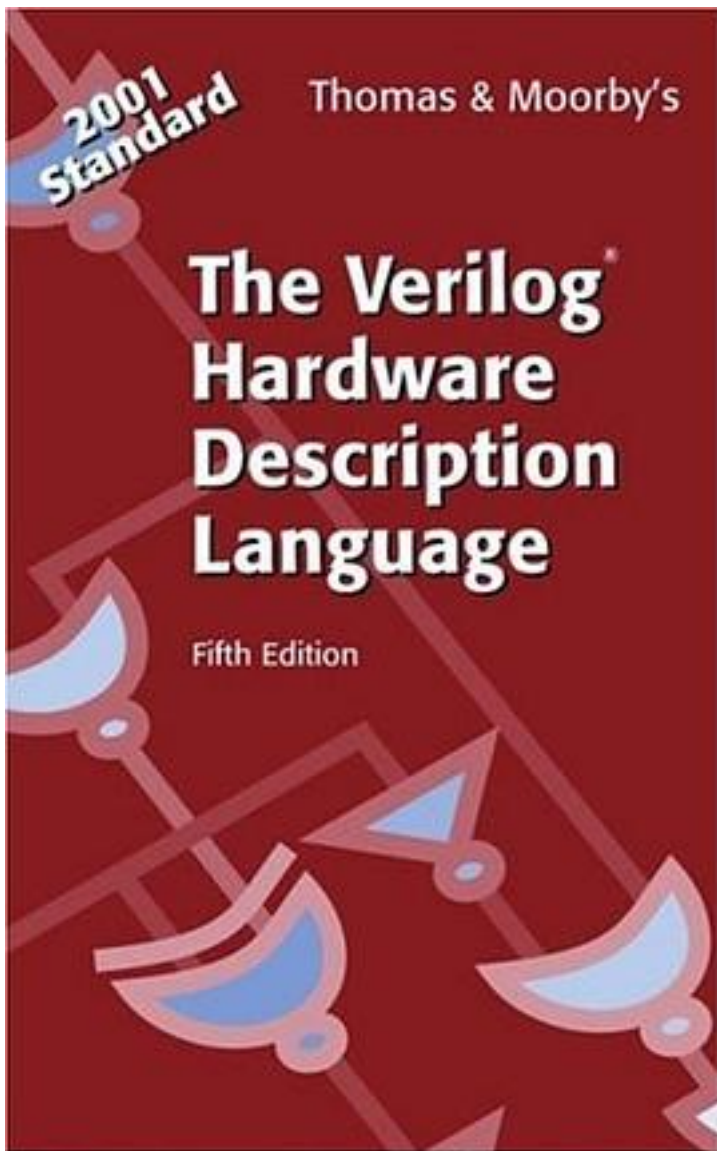
The Verilog® Hardware Description Language_下载链接1_

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Thomas & Moorby's The Verilog Hardware Description Language has become the standard reference text for Verilog. This edition presents the new IEEE 1364-2001 standard of the language. The examples have all been updated to illustrate the new features of the language. A cross referenced guide to the new and old features is provided. Thus, designers already familiar with Verilog can quickly learn the new features. Newcomers to the language can use it as a guide for reading "old" specifications. The Verilog Hardware Description Language, Fifth Edition, is a valuable resource for engineers and students interested in describing, simulating, and synthesizing digital systems; the extensive number of simulatable examples and wide range of representation styles covered ensure its quick use in design. The book is also ready for use in university courses, having been used for introductory logic design and simulation through advanced VLSI design courses. An appendix with tutorial help and a work-along style is keyed into the introduction for new students. Material supporting a computer-aided design course on the inner working of simulators is also included.

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