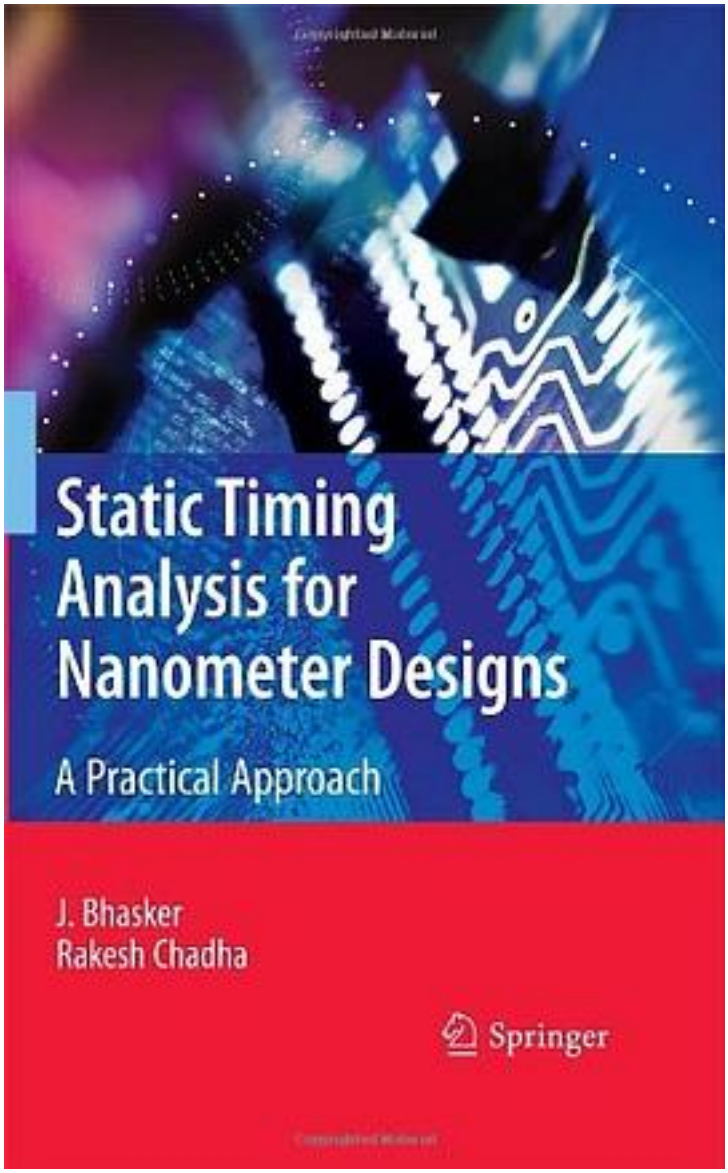
Static Timing Analysis for Nanometer Designs



Static Timing Analysis for Nanometer Designs_下载链接1_

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The book covers topics such as cell timing and power modeling; interconnect modeling and analysis, delay calculation, crosstalk, noise and the chip timing verification using static timing analysis. For each of these topics, the book provides a theoretical background as well as detailed examples to elaborate the concepts. The static timing analysis topics covered start from verification of simple blocks useful for a beginner to this field. The topics then extend to complex nanometer designs with in-depth treatment of concepts such as modeling of on-chip variation, clock gating, half-cycle paths, as well as timing of source-synchronous interfaces such as DDR. The impact of crosstalk on timing and noise is covered as is the usage of hierarchical design methodology. This book addresses CMOS logic gates, cell library, timing arcs, waveform slew, cell capacitance, timing modeling, interconnect parasitics and coupling, pre- and post-layout interconnect modeling, delay calculation, specification of timing constraints for analysis of internal paths as well as IO interfaces. Advanced modeling and analysis concepts such as controlled current source timing and noise models for nanometer technologies, power modeling including active and leakage power, crosstalk timing and crosstalk glitch calculation, verification of half-cycle and multi-cycle paths, false paths, synchronous interfaces are also covered.

作者介绍:

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标签

IC

STA

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本门内功

评论

算是STA方面的九阴真经了吧。

第8、第9章对我的帮助非常大，好多例子值得仔细研究。

重读无数遍了，再读一遍

实战性很不错。很久很久之后标记的一本书居然是学习教材。。。

STA宝典，再看一遍

当时作为做综合的一本参考进行了阅读 讲的还是比较细比较清楚 内容适合于初学者 可以跟design compiler的user guide配合一起看

对STA的了解就是从这本书开始，只可惜没有吃透。。

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书评

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