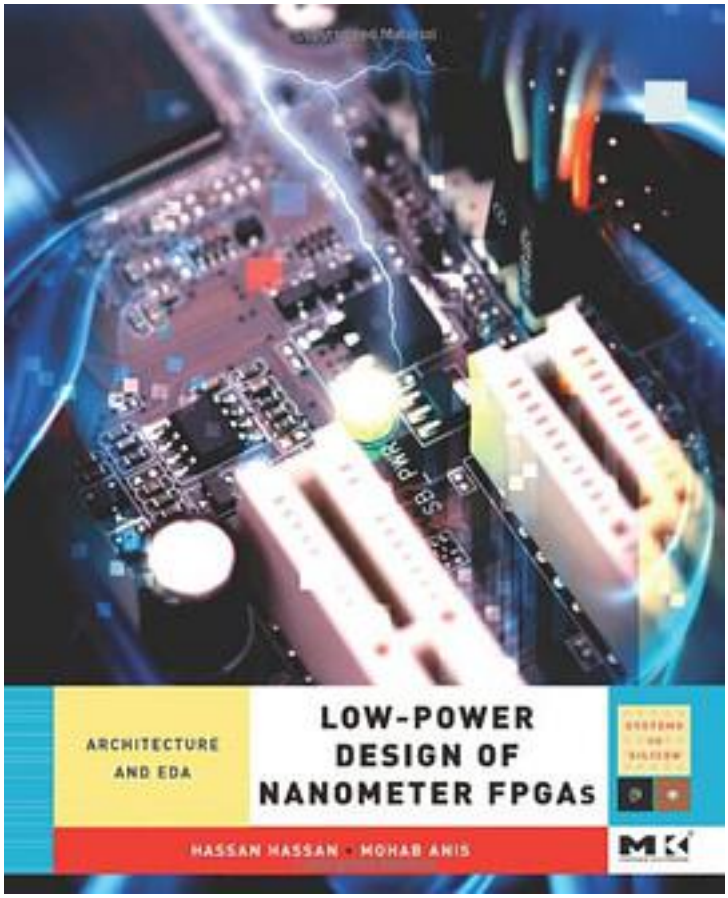
Low-Power Design of Nanometer FPGAs



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著者:Hassan, Hassan/ Anis, Mohab

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Low-Power Design of Nanometer FPGAs Architecture and EDA is an invaluable reference for researchers and practicing engineers concerned with power-efficient, FPGA design. State-of-the-art power reduction techniques for FPGAs will be described and compared. These techniques can be applied at the circuit, architecture, and

electronic design automation levels to describe both the dynamic and leakage power sources and enable strategies for codesign.

Low-power techniques presented at key FPGA design levels for circuits, architectures, and electronic design automation, form critical, "bridge" guidelines for codesign

Comprehensive review of leakage-tolerant techniques empowers designers to minimize power dissipation

Provides valuable tools for estimating power efficiency/savings of current, low-power FPGA design techniques

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