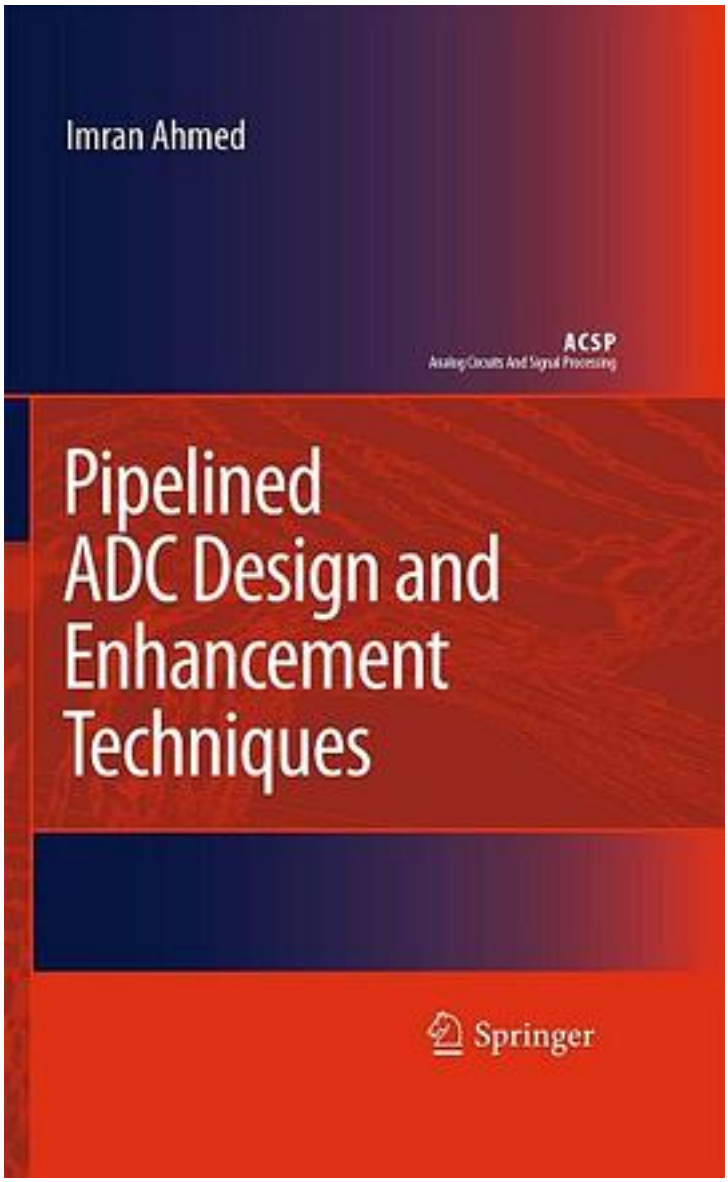
Pipelined Adc Design and Enhancement Techniques



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Pipelined ADCs have seen a tremendous growth in innovation and scope over the past few years. As such understanding both the basic concepts and the leading edge techniques required to realize pipelined ADCs which meet the challenging specifications of today’ s market and applications is required. While pipelined ADCs are popular circuit blocks, beyond publications in periodicals there are only a few condensed resources which are dedicated to education in the area. This book aims to help bridge the gap with a thorough discussion of pipelined ADCs.

This book is targeted to both the beginner and expert looking to acquire knowledge in pipelined ADCs. In the first section of this book, a tutorial discussion of several key design tradeoffs involved in designing a pipelined ADC is given. The discussion is presented with sufficient detail so as to allow those with only introductory knowledge of pipelined ADCs to quickly understand the limiting factors which motivate research into methods which enhance the performance of pipelined ADCs. In the second half of this book a detailed overview and discussion of four state-of-the-art pipelined ADCs with silicon implementations and measured results is given. The innovations include: a technique to rapidly digitally correct gain +DAC errors in a pipelined ADC, an architecture to enable a single ADC to be designed to achieve low power for a very wide range of sampling rates, a circuit technique to eliminate front-end sample-and-holds in pipelined ADCs, and finally a very low power pipelined ADC architecture based on capacitive charge pumps. The innovations presented in this book provides several tools which can be of great use to help a pipelined ADC designer deliver a design with good linearity, broad application, and very low power.

作者介绍:

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